ABSTRACT:

The present invention relates to a multi-processor computer system comprising

- at least two processors for parallel execution of processes,
- at least two cache memory units, each being associated with and connected to a separate processor,
- a connection bus connecting said processors and said cache memory units, and
- a process list unit connected to said connection line for storing a process list of processes to be available for execution by said processors.

In order to enable power saving if no processes for execution are available while guaranteeing a fast wake-up procedure if such processes are available it is proposed according to the present invention that said processors are adapted for loading a global wake-up variable signalling process additions of processes to said process list into their associated cache memory unit, for switching into a low-power mode if said process list contains no process for execution by said processors and for switching into a normal-power mode if said wake-up variable signals an addition of a process to said process list.

Thus, according to the present invention the cache coherence protocol is used for communicating and signalling the availability of processes for execution.

(Fig. 3)